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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,287	07/07/2003	Kunal R. Parekh	M122-2260	8293

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EXAMINER	
TSAI, H JEY	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 03/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,287	PAREKH ET AL.	
	Examiner	Art Unit	
	H.Jey Tsai	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-70 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-70 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 07 July 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-11, 47-50 are rejected under 35 U.S.C. § 102(b) as being anticipated by Kim 5,387,533.

Kim discloses a method of forming a DRAM device on the semiconductor substrate, which includes :

providing a semiconductor substrate 21 comprising a first pair of word lines 24 having a bit node received there between and a second pair of word lines 24 having a capacitor node received therebetween, see figs. 3-4+ and col. 4, lines 23+,

commonly forming a bit node contact opening within insulative material 28 over the bit node 26 and a capacitor node 26 contact opening within insulative material 28 over the capacitor node 26, fig. 4b, col. 5, lines 1+,

commonly forming sacrificial plugging material 29 within the bit node contact opening and within the capacitor node contact opening, col. 5, lines 29+, fig. 4d-4e,

removing sacrificial plugging material 29 from the bit node contact opening while leaving sacrificial plugging material within the capacitor node contact opening,

replacing the removed sacrificial plugging material 29 from the bit node contact opening with conductive material 30 that is in electrical connection with the bit node26,

after the replacing, forming the conductive material 30 into a bit line.

Claims 1-3, 8-16, 22-28, 34-38, 44-70 are rejected under 35 U.S.C. § 102(b) as being anticipated by Jeng 6,177,695.

Jeng discloses a method of forming a DRAM device on the semiconductor substrate, which includes :

providing a semiconductor substrate having a memory array area and a peripheral circuitry area peripheral to the memory array area, the substrate comprising a first pair of word lines (gate electrode 22 on left hand side of figures) having a bit node received therebetween, the bit node being received within the memory array area, figs. 2a+ and col. 3, lines 36+,

commonly forming a bit node contact opening (left hand side of figures) within insulative material 31/32 over the bit node, a first peripheral contact opening (right hand side of figure, such as fig.2K, see col. 3, lines 50+) within insulative material 31/32 over a first node in the peripheral circuitry area, and a second peripheral contact opening within insulative material over a second node in the peripheral circuitry area,

forming sacrificial plugging oxide material 53/61 within the bit node contact opening having a bit line 51/52, the first peripheral contact opening and the second peripheral contact opening, col. 4, lines 25+,

removing sacrificial plugging oxide material 61from the bit node contact opening, the first peripheral contact opening and the second peripheral contact opening, and replacing it with conductive material 111 that is in electrical connection with the bit line and bit node 51/52, the first node and the second node, fig. 2j-2k and col. 5, lines 23+,

after the replacing, forming the conductive material 111 into a bit line 51/52 in electrical connection with the bit node (diffusion region of gate transistor) and into a local interconnect line 111/112 in the peripheral circuitry area electrically interconnecting the first and second nodes,

after forming the bit line51/52, removing sacrificial plugging material 61 from the capacitor node contact opening. ss figs. 2f-2k.

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-70 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim1 of U.S. Patent No. 6,589,876. Although the conflicting claims are not identical, they are not patentably distinct from each other because removing material from bit line plug opening is a equivalent to removing a sacrificial plug, from bit line plug opening, and forming an opening over the a second substrate diffusion region is equivalent to a sacrificial plug in the second substrate diffusion opening for memory/capacitor electrode is removed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 12 and 51-52 are rejected under 35 U.S.C 103 as being unpatentable over Kim as applied to claims 1, 3-11, 47-50 above, and further in view of Jeng 6,177,695.

The difference between the references applied above and the instant claim(s) is: Kim teaches planarizing the sacrificial plug and insulative layer and forming a bit line contact after replacing sacrificial plug but does not using polishing to planarized the surface and using oxide layer as sacrificial plug. However, Jeng teaches at col. 4, lines 35-45 and figs. 2c-2e that sacrificial oxide plug and insulative layer 53/42/51/41 are polished to form a sacrificial oxide plug 61.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by using polishing to planarized the surface and using oxide layer as sacrificial plug as taught by Jeng because different materials can be polished at same time to obtain planar surface for both oxide plug and insulative layer.

Claims 4-7, 17-21, 29-33 and 39-43 are rejected under 35 U.S.C 103 as being unpatentable over Jeng as applied to claims 1-3, 8-16, 22-28, 34-38, 44-70 above, and further in view of Kim 5,387,533.

The difference between the references applied above and the instant claim(s) is: Jeng teaches forming a bit line contact after replacing sacrificial oxide plug but does not using conductive material as sacrificial plug. However, Kim teaches at col. 5, lines 25-36 that sacrificial plug material is metal or doped polysilicon layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the above references' teachings by using conductive material such as metal or semiconductive material such as doped polysilicon layer as sacrificial plug as taught by Kim because conductive material has different etching selectivity from the insulative layer, so that the sacrificial plug can be easily removed.

Any inquiry of a general nature or clerical matters or relating to the status of this application or proceeding should be directed to the Group customer service whose telephone number is (703) 306-3329 and Fax number (703) 872-9306. Group receptionist telephone number 703-308-0956.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to H. Jey Tsai whose telephone number is (571) 272-1684. The examiner can normally be reached on from 7:00 Am to 4:00 Pm., Monday thru Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (571) 272-1679. The fax phone number for this Group is (703) 872-9306.

hjt

3/9/04

H. Jey Tsai
Primary Examiner
Patent Examining Group 2800